Simulation

The following content has been imported from Legacy Help systems and is in the process of being checked for accuracy.

**Function**

The Simulation panel allows you to browse the VHDL hierarchy of the active FPGA project currently under simulation. For each specific area of the hierarchy - testbench, design under test and component instantiations within the design - you can interrogate the values of local signals and variables, as well as control whether data for those signals is collected and corresponding waveforms displayed.

**Content and Use**

The panel is populated with design information upon entering a simulation session.
The field at the top of the panel is used to indicate the elapsed simulation time.

The value in brackets after the elapsed time is the Delta count, which represents the number of Delta steps encountered since the last update to the elapsed simulation time. The Delta count value will be incremented if code in the source VHDL documents is executed for a single simulation cycle - using the **Delta Step** command (available from the **Simulator** menu or **VHDL Tools** toolbar) - and there is no resultant update to the elapsed time. If time is updated, the Delta count will be reset to zero.

## VHDL Design Hierarchy

The **Hierarchical Scopes** region of the panel shows the VHDL design hierarchy for the project. An entry appears in the hierarchy if the corresponding VHDL source document includes signal and/or variable declarations.

At the top of the hierarchy is the top-level entity declared in the associated testbench file (**.VHDTST**). **Beneath this is the design under test (DUT), which is the top-level VHDL file** (**.VHD**), typically generated (upon VHDL compilation) from the top-level schematic sheet for the design. At the lowest level are the component instantiations within the design where, typically, the code for each is contained in an underlying VHDL file, which in turn can be part of a defined VHDL library (**.VHDLIB**).

## Watching Local Signals

As you click on an entry in the **Hierarchical Scopes** region, the **Local Signals** region of the panel will display a list of all signals and/or variables local to the associated VHDL source document, the inclusion of which is determined by the two check boxes at the bottom of the panel - **how signals** and **Show Variables** respectively. For example, clicking on the top-level testbench entry will populate the region with all signals declared in the testbench itself, as illustrated in the image below:

The **Local Signals** region of the panel can be thought of as a 'locals' watch list. Whereas the VHDL Watches panel can be used to globally keep watch across all signals in the design hierarchy, the **Local Signals** region allows you to concentrate a watch on just those signals and/or variables local to a specific area of the hierarchy.

For each signal entry, the panel lists the following information:

- **Name** - the name of the signal, as defined in the source code
- **Type** - the type of signal (e.g. std_logic, std_logic_vector)
- **Value** - the current value assigned to the signal.

A small icon to the left of the signal name is used to indicate the watch status for the signal - enabled or disabled - and also whether or not the waveform for the signal is added to the Waveform Analysis window:

- **Watch is enabled and the waveform for the signal will be displayed in the Waveform Analysis window**
- **Watch is enabled, but the waveform for the signal will not be displayed in the Waveform Analysis window**
- **Watch is disabled, but the waveform for the signal will be displayed in the Waveform Analysis window**
- **Watch is disabled and the waveform for the signal will not be displayed in the Waveform Analysis window**

As you step through the lines of code in the source VHDL documents (.VHD, *.VHDTST), the watch-enabled signals will be evaluated and the corresponding *Value field updated.

### Right-click Menu

Right-clicking in the **Local Signals** region of the panel will pop-up a menu providing the following commands:

- **Add Watch** - add the selected signal(s) as new watches to the VHDL Watches panel
- **Enable Watch** - enable watch for the selected signal(s). The VHDL Simulator will collect data for all watch-enabled signals and the signal values will be updated on the panel as you step-debug your code
- **Disable Watch** - disable watch for the selected signal(s). The VHDL Simulator will not collect data for watch-disabled signals and the signal values will not be updated on the panel as you step-debug your code
- **Add Waveform** - add the waveform(s) for the selected signal(s) to the Waveform Analysis window. The waveform(s) will be added to the top of the list of existing waveforms.
- **Delete Waveform** - delete the waveform(s) for the selected signal(s) from the Waveform Analysis window
- **Insert Wave View** - add an additional waveform view of the selected signal(s) to the Waveform Analysis window. The new waveform view(s) will be inserted above the currently selected signal waveform in the window
- **Remove Wave View** - remove all additional wave views for the selected signal(s) from the Waveform Analysis window
- **Focus Wave** - focus the corresponding waveform entry for the signal, in the Waveform Analysis window. The waveforms will be vertically scrolled, such that the chosen signal is shown as the first waveform entry below the analysis timeline.
- **Enable All Watches** - change the watch state for all signals listed in the panel to enabled
- **Disable All Watches** - change the watch state for all signals listed in the panel to disabled
- **Add All Waveforms** - add the waveforms for all signals listed in the panel, to the Waveform Analysis window
- **Delete All Waveforms** - delete the waveforms for all signals listed in the panel, from the Waveform Analysis window
- **Insert All Wave Views** - add an additional waveform view for all local signals whose waveform
has been added to the Waveform Analysis window. The new waveform view(s) will be inserted above the currently selected signal waveform in the window

- **Remove All Wave Views** - remove the additional wave views for all signals from the Waveform Analysis window

**Notes**

A VHDL simulation session is entered from either a VHDL source document (*.VHD) or VHDL testbench file (*.VHDTST), by using the **Simulate** command - accessed from either the **Simulator** menu or **VHDL Tools** toolbar.

- If you have multiple testbenches in your project, all will be compiled to produce the intermediate analyzed files (*.AN). **However, only the testbench document (and associated top-level entity therein) declared in the *Simulation** tab of the **Options for Project** dialog, will be used by the Elaborator to ultimately produce the simulation executable file (*.VX). It is this testbench that will be displayed in the **Hierarchical Scopes** region of the Simulation panel.

- When using the **Delta Step** command, it is possible that several simulation cycles may be run without the elapsed simulation time changing. This is due to the fact that some Delta steps can be infinitesimally small in their delay.

- The initial state of signals in the **Local Signals** region of the panel - with respect to watch state and waveform display is defined by the settings you choose in the **Edit Simulation Signals** dialog.
This dialog lists all of the signals in the design, in terms of blocks. The top block (with no name) represents the top-level signals contained in the testbench (which equate to the ports of the top-level schematic document, where one exists). Each block that follows represents the signals local to a component instantiation within the design.

The dialog will appear whenever you start a new simulation session or reset the current one. Top-level signals are, by default, all enabled for simulation and waveform display. Care should therefore be taken to set the entries in the dialog as required when restarting a current simulation, otherwise the default settings will be passed to the VHDL Watches panel and will override any particular watch/waveform state configuration you have previously defined.

- The **Value** field for a watch-enabled signal is updated after the line of code has been executed.
- Enabling the watch for a signal essentially specifies to the debugger that data for the signal is to be collected. If a signal is watch-disabled, but its waveform is added to the Waveform Analysis window, you will see an entry for the signal - its waveform cannot update as data is not being collected. Conversely, an watch-enabled signal that is not initially added to the Waveform Analysis window can be added at a later stage, as the data required for display has been collected and stored.
- Changes made to a signal in the Simulation panel, in terms of its enabled/disabled watch state and the addition of its waveform to the Waveform Analysis window, will be reflected in the VHDL Watches panel and also in the *Edit Simulation Signals* dialog.
Conversely, any changes made to a signal entry in the VHDL Watches panel, or an entry in the *Edit Simulation Signals* dialog, will be passed to the corresponding local signal entry in the **Local Signals** region of the Simulation panel.

- Standard **CTRL** + Click and **SHIFT** + Click functionality is supported for selection of multiple signals in the **Local Signals** region of the panel.
- The keyboard shortcuts **Up Arrow** and **Down Arrow** can be used to select the previous and next entry in a region of the panel, respectively.

**See Also**

- [Altium Designer Panels Reference](#)
- [Working with Panels](#)

*Source URL: https://techdocs.altium.com/display/ADRR/EditVHDL_Pnl-Simulation((Simulation))_AD*