The I2C Master Controller component (WB_I2CM) is used to facilitate data transfers over the I2C Bus and therefore ease communication with I2C devices external to the FPGA device. The I2C Bus is a two-wire, bi-directional serial bus that enables short distance data exchange between multiple devices connected to the bus.

Devices connected to the I2C bus can either be Master or Slave. The difference between the two lies primarily in the fact that a Master can take control of the serial clock and data lines (that constitute the I2C bus), changing their state in accordance with requests from the host processor.

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[www.semiconductors.philips.com/buses/i2c/licensing/index.html](http://www.semiconductors.philips.com/buses/i2c/licensing/index.html)

**Features at-a-glance**

- I2C version 2.1 standard compliance
  - Transmission speed modes:
    - Standard Mode (up to 100kb/s)
    - Fast Mode (up to 400kb/s)
High-speed Mode (up to 3.4Mb/s)

- Multimaster Mode
- 7-bit slave addressing
- Wishbone-compliant

**Availability**

From an OpenBus System document, the I2C Master Controller component can be found in the **Peripherals** region of the **OpenBus Palette** panel.

From a schematic document, the WB_I2CM component can be found in the FPGA Peripherals (Wishbone) integrated library (FPGA_Peripherals_Wishbone.IntLib), located in the \Library\Fpga folder of the installation.

**Designing with the WB_I2CM**

Use the following links to explore use of the WB_I2CM in more detail:

- [Pin Description](#)
- [Operational Overview](#)
- [Block Diagram](#)
- [Accessible Internal Registers](#)
- [Defining the Frequency of SCLK](#)
- [Host to Controller Communications](#)

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